

# AUA234CI3 Intelligent All-Rate DS0 Dataport

(For use in SLC<sup>®</sup>-5/SLC-2000-type Shelves)

CLEI\* Code: 5SC6STSBAA

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## 1. GENERAL

### 1.1 Document Purpose

This practice describes the Westell AUA234C Issue 3 Intelligent All-Rate DS0 Dataport Unit for use in SLC<sup>®</sup>-5/SLC-2000-type shelves. Figure 1 shows the front panel of the AUA234CI3.

- NOTE -  
Hereafter the AUA234CI3 Intelligent All-Rate DS0 Dataport Unit may be referred to as the "DS0-DP" or "AUA."

### 1.2 Document Status

Whenever this practice is updated, the reason will be stated in this paragraph. The Issue 3 equipment improves the module's loopback performance when used in the tandem configuration. There are no changes to features or functions.

### 1.3 Product Purpose and Description

Westell's Intelligent All-Rate DS0 Dataport, Model AUA234C Issue 3, provides DS0 access to the Digital Data System (DDS), Switched-56 and other compatible networks, through Lucent SLC-5, SLC-2000, or Westell IDB5000 terminal assemblies. The unit provides a 64 kb/s DS0 interface for rates of 2.4, 4.8, 9.6, 19.2<sup>1</sup>, 38.4, 56, and 64 kb/s, and secondary channels. Switch-selected options for subrate error correction, latching loopback, and zero code suppression, are also provided. All switch options are either remotely provisioned through the DS0 channel, or locally provisioned with option switches. The AUA234CI3 provides DDS test capability that is compatible with industry standard test equipment and procedures.

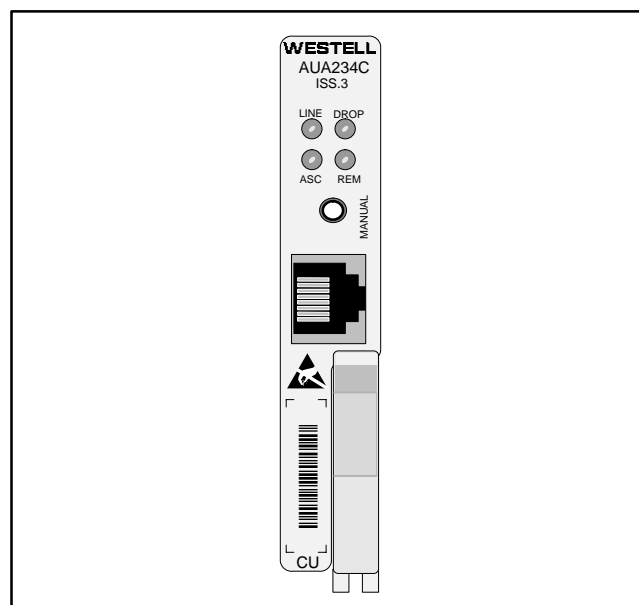


Figure 1. Front View of AUA234CI3

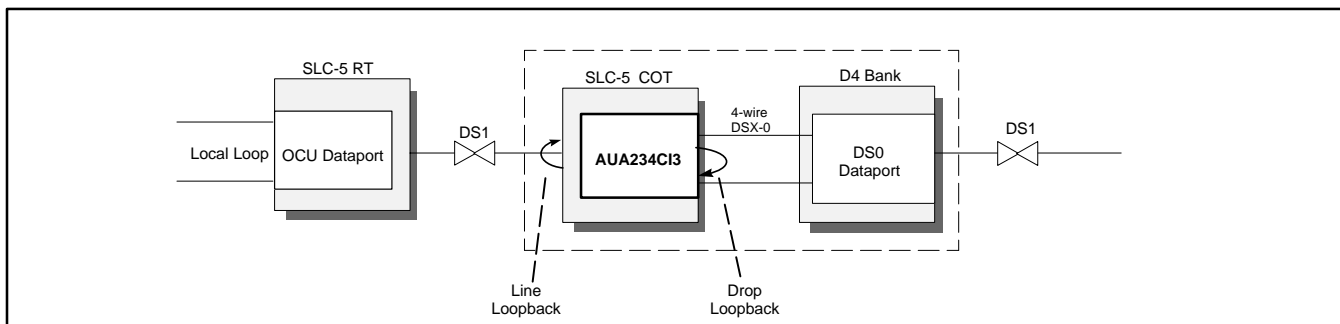
### 1.4 Product Mounting

The AUA mounts in a single channel unit position of a SLC-5 or SLC-2000 assembly (or a Westell IDB5000 Series terminal assembly) and provides the interface between the DSX-0 loop and the channel bank's common equipment.

### 1.5 Product Features

Features of Westell's AUA are as follows:

- Compatible with existing Digital Data System (DDS) equipment, Basic Dedicated Digital Service (BDDS), and Switched-56 Service
- Provides 2.4, 4.8, 9.6, 19.2, 38.4, 56, and 64 kb/s service rates
- Switch-selected error correction for all customer service rates
- Latching loopback option
- Front-panel DS0 (Drop) and DS1 (Line) loopback control
- Zero Code Suppression option
- Front panel REM LED to indicate a remotely provisioned unit



**Figure 2. Network Application**

- Meets or exceeds TA-TSY-000077 and TR-NPL-000157 technical requirements
- Compatible with in-band control of intelligent DDS channel equipment
- Low power consumption
- 7-year warranty

## 2. APPLICATIONS

The AUA is designed for DS0 and tandem terminal applications to provide access to digital data networks via digital loop carrier facilities. The unit mounts in a single channel unit position of Lucent SLC-5, SLC-2000, or Westell IDB5000 Series Central Office Terminal assemblies and provides the interface between the DSX-0 loop and the channel bank's common equipment. The unit supports all service rates, including switched 56 kb/s operation.

### 2.1 Error Correction

The DS0-DP is equipped to provide error correction at all customer service rates to ensure acceptable data error rates on the DS1 facility. For subrate data up to 9.6 kb/s, error correction is based on a majority count of the byte-stuffed data. At 19.2, 38.4, 56 and 64 kb/s, error correction is based on parity bytes that are generated using the BCH coding scheme and transmitted with the data. At 38.4, 56, and 64 kb/s the parity byte is transmitted in a separate DS0 channel from the data. The parity byte channel is in the even channel following the data. Error correction for sub-rates 38.4, 56, and 64 kb/s data can be disabled when desired.

### 2.2 Loopback

The DS0-DP provides latching DS0 (Drop) or DS1 (Line) loopback to facilitate testing and troubleshooting in isolating the source of a failure. The loopback functions are controlled by network control codes transmitted from the Serving Test Center (STC), or from the front panel of the unit.

#### 2.2.1 DS0 Latching Loopback (Drop Loopback)

As shown in Figure 2, the DS0 (Drop) loopback mode isolates the DSX-0 signaling from the network by providing a loopback point at the DS0 interface of the DS0-DP. When DS0 (Drop) loopback is activated, the unit's receive output is looped back to its transmit input and connections to the DSX-0 loop are open. DS0 (Drop) loopback is deactivated with a release code.

#### 2.2.2 DS1 Latching Loopback (Line Loopback)

As shown in Figure 2, the DS1 (Line) loopback mode isolates the DS1 signal from the network by providing a loopback point at the DS1 interface of the DS0-DP. When DS1 (Line) loopback is activated, the unit's DS1 transmit signal is looped back to its DS1 receive input. DS1 (Line) loopback is deactivated with a release code from the STC.

## 3. FUNCTIONAL OPERATION

Refer to Figure 3 as needed while reading the following functional description.

The AUA234CI3 DS0-DP provides an interface between a DSX-0 cross-connect frame (64 kb/s, bipolar, NRZ signals) and the common equipment of a COT assembly.

The transmit-side circuitry of the DS0-DP converts bipolar DS0 signals received from the DSX-0 cross-connect frame to the unipolar format used internally by the channel bank. The receive-side circuitry performs the reverse of these functions, converting the unipolar signals received from the common equipment to the bipolar format used at the DSX-0 frame. At the common equipment (DS1) interface, the transmit and receive bus interface circuits decode the time slot window from the common control signals and provide access to the terminal data buses for the formatted DS0 signals at the appropriate time. The formatted signals are bussed to the common equipment on the TPCM (transmit) and RPCM (receive) leads.

Phase synchronization between the DSX-0 signals at the drop ports and the formatted DS0 signals at the line ports is provided by the microprocessor transmit and receive speed buffers. These elastic storage registers compensate for any phase differences between the DS1 clock signals on the TCLK and RCLK leads and the 64 kb/s byte clock from the composite clock circuit.

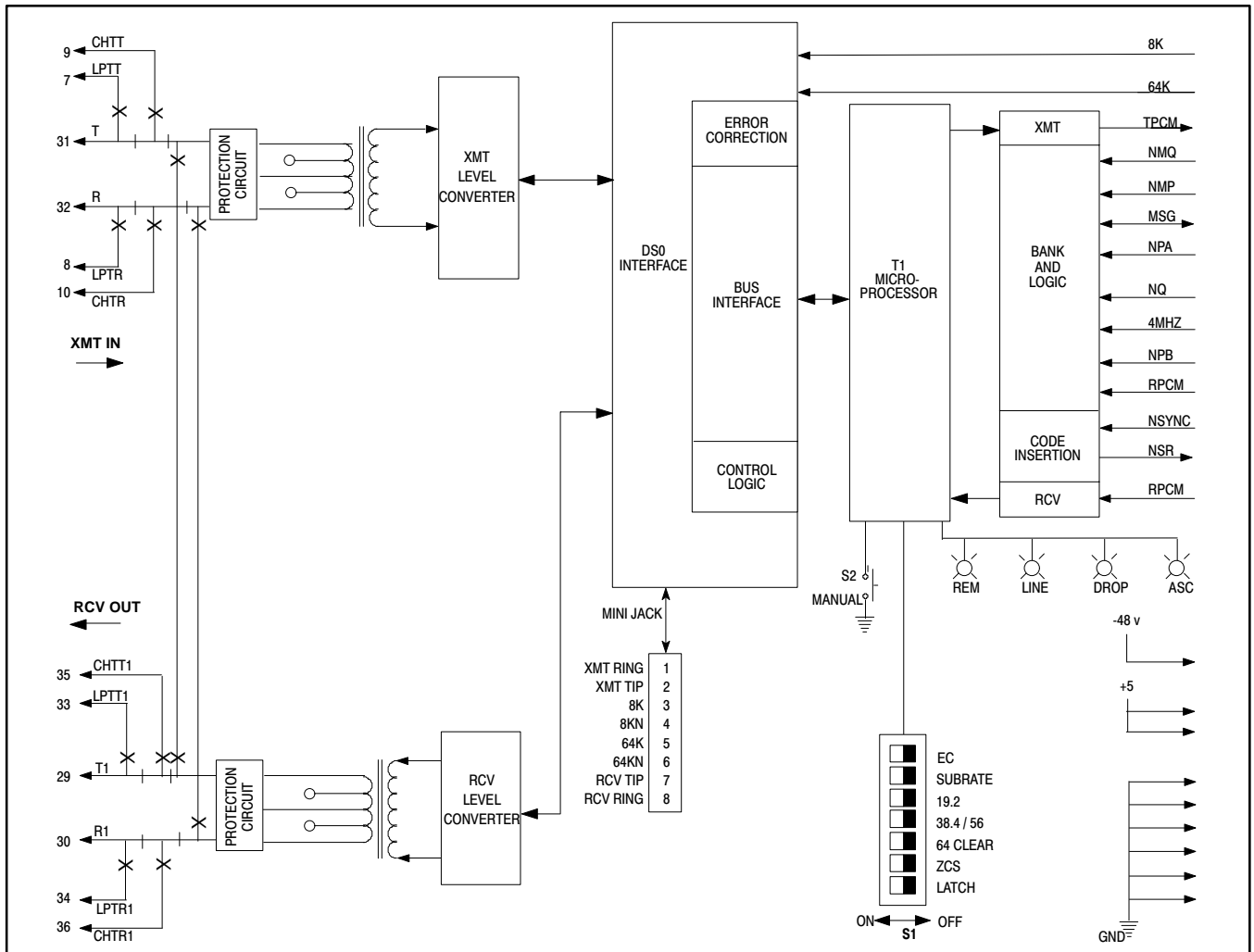


Figure 3. Functional Diagram

BYTE POSITION	DS0-A	DS0-B
1	data-1	unassigned mux
2	data-2	data-1
3	parity-1	data-2
4	parity-2	unassigned mux
5	parity -2 complement	unassigned mux

Table 1. Network 19.2 Kb/s Byte Block Format

Data network synchronization for the DS0-DP is derived from the system composite clock signal that generates 8 kb/s byte and 64 kb/s bit clock on the backplane. The DDS clock signals consist of integrated bit (64 kb/s) and byte (8 kb/s) clock signals that are supplied from a local source for externally timed channel banks or derived from the received DS1 bit stream for loop timed channel banks.

### 3.1 Loopback

Loopback on the DS0-DP is activated from the latching loopback sequence within the DS0 channel. Signal loopback towards the carrier, looped at the metallic DSX-0 points, will occur when the unit is placed in DS0 (Drop) loopback. The signal loopback is towards the DSX-0, looped at the DS1 point, when the unit is in DS1 (Line) loopback. Loopback remains active until a valid disconnect sequence is received.

### 3.2 Switched-56 Operation

A 56 kb/s station advances on-hook signaling by sending Control-Mode-Idle (CMI) transmission signals and off-hook signaling by sending Data-Mode-Idle (DMI) transmission signals. The unit operates with a SLC-5 OCU-DP (e.g., Westell's AUA252C) to provide Switched-56 connectivity.

### 3.3 Error Correction

The DS0-DP provides majority logic error correction for sub-rate data up to 9.6 kb/s. The unit takes advantage of byte-stuffed

rate matching to implement majority logic error correction on the transmit side. To match the 64 kb/s DS0 rate, subrate data bytes are repeated 5, 10, or 20 times for customer data rates of 9.6, 4.8, and 2.4 kb/s respectively. The DS0 at the other end of the circuit compares the repeated bytes to derive an error corrected signal. Error correction at all rates can be disabled when desired.

The DS0-DP provides parity byte error correction for 19.2, 38.4, 56 and 64 kb/s data. Parity bytes are formed by the Microprocessor using the BCH parity code. At 19.2 kb/s, parity bytes are sent with the data bytes (i.e., in the same DS0 channel time slot). Since the microprocessor must arrange subrate DS0 bytes into 5-byte blocks to accommodate majority logic error correction, it is convenient to do the same for 19.2 kb/s DS0-A and DS0-B bytes. Therefore, in the 19.2 kb/s DS0-A byte format (error corrected) data is sent in the following manner: two data bytes, two parity bytes (one for each data byte), and a synchronization byte (which is the complement of the second parity byte and is used to mark the end of the five-byte block). In the 19.2 kb/s DS0-B byte format (no error correction), data is sent as follows: unassigned mux, two data bytes (with most significant bits having leading 1's used for synchronization), and two unassigned mux bytes (see Table 1). Due to bandwidth limitations, parity bytes for 38.4, 56 and 64 kb/s data must be sent in a separate DS0 channel time slot from the data bytes. The parity byte is assigned to the EVEN channel immediately following the ODD data channel.

### 3.4 Databus Interface

The processed data is clocked out of the microprocessor into the Speed Buffer. This buffer is an elastic register that phase synchronizes the data bytes to the framed PCM DS0-A channel. The synchronized bytes are read out of the DS0-DP to the channel bank common equipment interface circuit. The XMT Bus Interface circuit contains the necessary logic to generate the transmit time slot window and the common control channel unit identification.

### 3.5 Receive Path (Network to Customer)

The receive path of the DS0-DP operates in essentially the reverse of the transmit path; 64 kb/s DS0 bytes from the common equipment are converted to DSX-0 signals. The 64 kb/s DS0 bytes are read into the DS0-DP channel unit via the RDATA lead under control of the RCV Bus Interface circuit. The RCV Bus Interface circuit contains the logic required to generate the receive time slot window and common control channel unit identification. The received DS0 bytes are applied to the Code Insertion circuit, which also monitors the CGA STATUS from the common equipment. If the CGA signal is a logic 1 (indicating the channel bank has lost synchronization to the DS1 bit stream) a MUX-OUT-OF-SYNC code is sent towards the DSX-0 interface. Otherwise, the DS0 bytes are applied to the Error Correction circuit.

### 3.6 Receive Error Correction

Error correction on the DS0-DP is controlled by the Microprocessor. The Microprocessor automatically sets the Error

Correction circuit to provide majority logic or parity byte error correction - depending on the selected customer service rate. Majority logic error correction used for subrate data up to 9.6 kb/s is based on a best 3-out-of-5 byte voting scheme. The microprocessor locates and marks the boundaries of the 5-byte blocks of received data used for the majority count, and the Error Correction circuit outputs a single-corrected byte. Error correction at all speeds can be disabled when desired.

Parity byte error correction, used for 19.2, 38.4, 56 and 64 kb/s data, is based on BCH encoded parity bytes. Parity bytes for 19.2 kb/s data are located by the microprocessor using a synchronization byte sent from the distant DS0. The location of the parity byte for 56 and 64 kb/s data, is in the EVEN channel following the data time slot.

### 3.7 Latching Loopback

The DS0-DP also provides a latching loopback function for both DS0 (Drop) and DS1 (Line) loopback points. Latching loopback allows use of codes other than the standard loopback codes for circuit testing. Latching loopback is activated and deactivated by the predefined control code sequences sent from the network. Latching loopback control code sequences are given in Table 2.

ENABLE SEQUENCE	BYTES SENT	BYTE NAME	NETWORK CODE
1	30-45	Transition in progress (TIP)	*S011110
2	30-45	DS0/DS1 loopback	S0000101
3	100-200	loopback enable (LBE)	S1010110
4	10-40	Far End Voice (FEV)	S1011010
DISABLE	35-40	Transition in Progress (TIP)	S0111010

\*S = Subrate framing bit; not used for detection of the DS0 code.

**Table 2. Latching Loopback Codes**

### 3.8 Channel Unit Common Circuitry Timing

Data network synchronization for the DS0-DP is derived from the composite clocks on the backplane. The composite clock signal consists of integrated bit (64 kb/s) and byte (8 kb/s) clock signals. The composite clock signal can be supplied from a local source for externally timed channel banks or from the received DS1 bit-stream for loop-timed channel banks. The bit and byte components of the clock signal provide synchronization to the data network.

### 3.9 Carrier Group Alarm (CGA)

The DS0-DP sends the MUX-OUT-OF-SYNC code towards the DSX-0 interface when a disruption of service occurs on the DS1 interface. The service disruption is caused by an out-of-frame condition in the channel bank equipment.

## 4. INSTALLATION

- NOTE -

The central office terminal requires an AUA3 OTU Office Timing Unit clocked by a composite clock signal from an office timing reference, preferably a Building Integrated Timing Supply (BITS).

- INSPECTION NOTE -

Visually inspect the unit for damages prior to installation. If the equipment was damaged in transit, immediately report the extent of the damage to the transportation company and to Westell (see Part 8 for telephone number).

- PRECAUTIONARY STATEMENT -

Never install telephone wiring during a lightning storm.  
Never install telephone jacks in wet locations unless the jack is specifically designed for wet locations.  
Never touch uninsulated telephone wires/terminals unless the telephone line is disconnected at the network interface.  
Use caution when installing or modifying telephone lines.



**CAUTION - STATIC-SENSITIVE**



This product contains static-sensitive components! Proper electrostatic discharge procedures must be followed to maintain personal and equipment safety. Do not store near magnetic, electromagnetic or electrostatic fields. Always store or ship units in the original static-protective packaging.

### 4.1 Mounting Location

The AUA234CI3 mounts in one channel unit position of Lucent SLC-5, SLC-2000 or Westell IDB5000 Series Central Office Terminal (COT) assemblies, or the equivalent.

- NOTE -

The DSX-0 interface is designed for intrabuilding use only, not for direct connection to outdoor facilities.

- CAUTION -

Use care when installing and removing modules - do not force a module into place. If a module resists insertion, remove it and check for obstructions in or near the connectors and mounting slots. The module may then be carefully aligned and gently re-inserted.

### 4.2 Installer Connections

Installer connections to the DSX and carrier are made via the connectorized cables of the SLC-5, SLC-2000, or IDB5000 COT assembly. All other connections required by Westell's AUA234CI3 including power, are integral to the channel bank assembly.

## 5. PROVISIONING

The AUA234CI3 is provisioned either remotely through the DS0 channel or locally with option switches. A front panel LED displays the remote (REM) provisioning status. The unit contains option switches that condition the unit for proper

operation in a given application. All options should be set according to the WORD document.

### 5.1 Local/Remote Provisioning

Depress the front panel **MANUAL** push button for more than 3 seconds to toggle between **local** or **remote** provisioning. All options are programmed by switches or optioned through the network DS0 channel. The REM LED is off when locally optioned. If the unit is remotely optioned and later optioned locally, the remote options can be restored depressing the **MANUAL** switch for more than 3 seconds. The REM LED should turn on. (The factory default is *local* provisioning.)

### 5.2 Local Provisioning

To provision the unit locally, set the switch options on the board. As described in Figure 4 and Table 3.

#### 5.2.1 Error Correction

Set Switch S2-1 to the ON position to enable error correction for any of the selected rates. Set the system for error correction with the CRAFT INTERFACE UNIT when a second time slot is required for error correction, such as with 38.4, 56, and 64 kb/s rates.

#### 5.2.2 Subrate

Set Switch S2-2 to the ON position to enable subrate operation of 2.4, 4.8, and 9.6 kb/s rates.

#### 5.2.3 19.2 Kb/s Rate

Set Switch S2-3 to the ON position to enable 19.2 kb/s rate operation.

#### 5.2.4 38.4 / 56 Kb/s Rate

Set Switch S2-4 to the ON position to enable rate operation of 38.4 kb/s or 56 kb/s.

#### 5.2.5 64 Kb/s Rate

Set Switch S2-5 to the ON position to enable 64 kb/s rate operation.

#### 5.2.6 Zero Code Suppression (ZCS)

When Switch S2-6 is set to OFF, the AUA234CI3 allows eight consecutive zeros to be transmitted to the carrier. If zero code suppression is set to ON, a string of eight zeros is encoded to ensure adequate 1's density in the network's DS1 facility. Zero code suppression is automatically disabled for 56 kb/s with secondary channel and 64 kb/s channel services.

#### 5.2.7 Latching Loopback

Set Switch S2-7 to the ON position to enable latching loopback capability.

### 5.3 Remote Provisioning

Remote provisioning is accomplished with distinct DS0 codes when the DS0-DP is in the command mode. Remote provisioning is activated by a sequence of DS0 bytes that are similar to the Bellcore defined latching loopback sequence. Once in this mode, provisioning is controlled and status is accessed with an in-band data-link between the remote test equipment (e.g. TPI 108/109 RT II) and the microprocessor in the AUA234CI3. The front panel REM LED indicates a remotely provisioned unit.

#### 5.3.1 Inventory Information

The following information is available directly from a remote menu:

- Device type
- CLEI Code
- Part Number
- Revision Number
- Serial Number

#### 5.3.2 Remote Provisioning

The following items can be remotely provisioned directly from a remote menu:

- Data Rate — Sub (2.4, 4.8, 9.6), 19.2, 38.4, 56, 64
- Error Correction — on/off
- Zero Code Suppression— on/off
- Latching loopback — on/off

#### 5.3.3 Diagnostics

The following information is available directly from a remote menu:

- T1 Out-of-Frame — yes/no
- T1 Out-of-Frame count
- Nonvolatile Memory Failure — yes/no
- Configuration Invalid — yes/no
- New Device — yes/no
- Device Self Test — pass/fail
- Clear New Device State
- Clear Status Report
- Reset Device
- ALL ZEROS

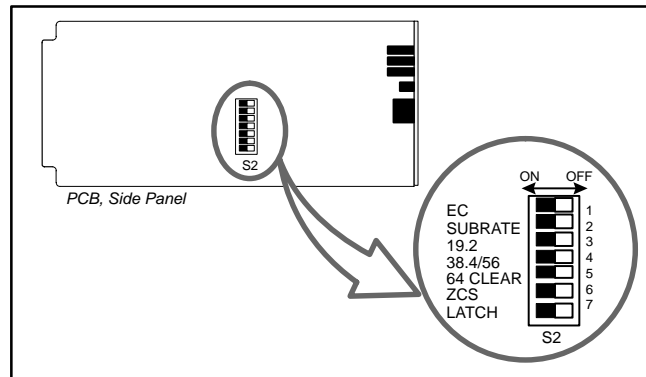


Figure 4. 7-Segment Option Switch, S2

Switch # and Label	Position	Function
S2-1 EC	ON	Enables Error Correction
	OFF	Disables Error Correction
S2-2* SUBRATE	ON	Enables Subrate Operation (2.4, 4.8, 9.6 kb/s)
	OFF	Disables Subrate Operation
S2-3* 19.2	ON	Enables 19.2 kb/s Rate Operation
	OFF	Disables 19.2 kb/s Rate Operation
S2-4* 38.4/56	ON	Enables 38.4 or 56 kb/s Rate Operation
	OFF	Disables 38.4 or 56 kb/s Rate Operation
S2-5* 64 CLEAR	ON	Enables 64 kb/s Rate Operation
	OFF	Disables 64 kb/s Rate Operation
S2-6 ZCS	ON	Enables ZCS to prevent all zeros toward network, normally set to "ON" for 56 kb/s (without secondary channel) and lower rates
	OFF	Disables ZCS to allow all zeros toward network (ZCS is automatically disabled for 56 kb/s with Secondary Channel and 64 kb/s rates)
S2-7 LATCH	ON	Enables Latching Loopback
	OFF	Disables Latching Loopback

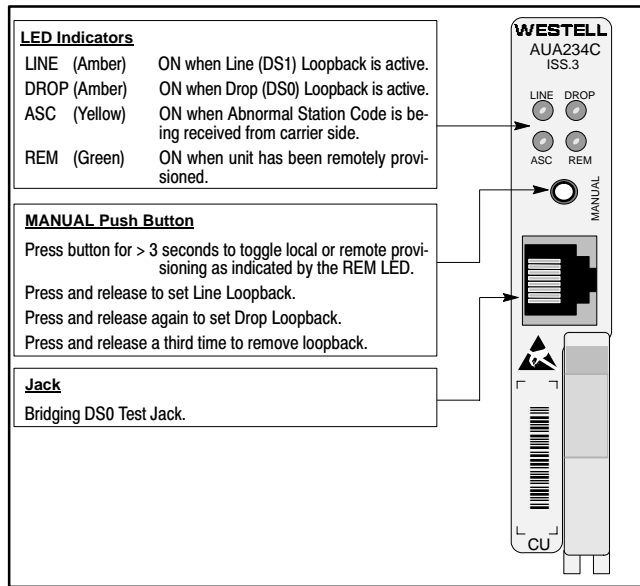
\* Only one rate switch (S2-2 thru S2-5) can be set to ON for a given application.

Table 3. S2 Option Switch Settings

### 5.4 Channel Bank Provisioning

Channel slot provisioning information, entered through a Craft Interface, is required by the SLC-5 or SLC-2000 system to allow the channel unit to be recognized and operate properly. Through the Craft Interface, address the appropriate system, terminal, and slot number, and enter the following information:

- Enter the **CLEI** as **5SCU38**. This code is used, rather than the AUA234CI3's actual CLEI, in order for the SLC-2000 system to recognize the unit as an DS0-DP.
- Select a **Function Code**, **DS0A** or **DS0B**.
- Select the type of **Error Correction** desired, e.g., **SCEC**, **MVEC**, **19.2EC** or **NONE**. This provisions the channel bank



**Figure 5. Front Panel Operation**

to support the correct number of slots for error correction, but does not affect the actual operation of the AUA234CI3.

- Enter a value of **YES** or **NO** for **All Zero Code Allowed**. The value is not used by the AUA234CI3.
- Enter a value of **YES** or **NO** for the Redline option.

## 5.5 Clear Channel Capability

When the AUA234CI3 is used in the 64 kb/s mode of operation, it is required that the Carrier System be equipped with a Line Interface Unit (LIU) capable of B8ZS operation to allow unconstrained clear channel capability.

## 6. FRONT PANEL OPERATION

Please see Figure 5 for a description of the AUA234CI3's front panel operation.

## 7. TESTING

Initial testing consists of performing the standard test procedures for DDS dataport channel units using the KS-20908 and KS-20909, or the TPI 108/109, or equivalent, receiver and transmitter data test sets. These procedures are intended only to ascertain proper operation of the unit and, if problems should occur, to isolate those problems to the most probable area.

### 7.1 Front Panel Access

A modular mini-jack on the AUA234CI3 front panel provides DS0 bridging access for testing with standard DDS test equipment. Composite 8 kb/s and 64 kb/s clock signals, receive and transmit channel signals are brought out on the RJ48 jack for test set access. With respect to the AUA234CI3, "far" is towards the carrier, and "near" is towards the loop.

## 7.2 Trouble Reporting

If trouble is encountered, verify all installer connections to the assembly and check that the CO power fuse is not blown. Also verify all module connections and option switch settings, and verify the modules are making a positive connection with the shelf connector. If trouble persists, replace the suspect unit and repeat procedures outlined. These procedures are not designed to effect repairs or modifications. Any tests beyond those outlined herein, or repairs made beyond replacing a faulty unit, are not recommended and may void the warranty.

## 8. CUSTOMER & TECHNICAL SERVICES

If technical or customer assistance is required, contact Westell by calling or using one of the following options:

Voice: (630) 898-2500  
 Voice: (800) 323-6883  
 email: [global\\_support@westell.com](mailto:global_support@westell.com)

Visit the Westell World Wide Web site at <http://www.Westell.com> for additional information about Westell.

## 9. WARRANTY & REPAIRS

### 9.1 Warranty

Westell warrants this product to be free of defects at the time of shipment. Westell also warrants this product to be fully functional for the time period specified by the terms and conditions governing the sale of the product. Any attempt to repair or modify the equipment by anyone other than an authorized Westell representative will void the warranty.

### 9.2 Repair and Return

Westell will repair or replace any defective Westell equipment without cost during the warranty period if the unit is defective for any reason other than abuse, improper use, or improper installation. Before returning the defective equipment, first request a Return Material Authorization (RMA) number from Westell. Once an RMA number is obtained, return the defective unit, freight prepaid, along with a brief problem description, to:

Westell, Inc.  
 ATTN: R.G.M. Department  
 750 N. Commons Drive  
 Aurora, IL 60504-7940

Replacements will be shipped in the fastest manner consistent with the urgency of the situation. Westell will continue to repair or replace faulty equipment beyond the warranty period for a nominal charge. Contact Westell for details.

## 10. SPECIFICATIONS

The electrical specifications and the compliance/regulatory agency specifications are listed below, the ordering information is shown in Table 5, and the physical specifications are shown in Table 4.

Feature	U.S.	Metric
Height	3.59 in.	9.1 cm
Width	0.66 in.	1.68 cm
Depth	9.85 in.	25 cm
Weight (approx.)	5.8 oz.	164.4 g
Operating Temp.	32° to 122°F	0° to 50°C
Humidity	0 to 95% (no condensation)	

**Table 4. Physical Specifications**

**Electrical Specifications**

- A. **Network Interface:** 64 Kb/s DS0.
- B. **Service Rates:** 2.4, 4.8, 9.6, 19.2, 38.4, 56, and 64 kb/s
- C. **Duty Cycle Conversion:** Bipolar Non-Return-to-Zero (NRZ) to unipolar NRZ

- D. **Timing:** Derived from DDS composite clock (64 Kb/s and 8 Kb/s).
- E. **Pulse Amplitude:** Between 3.0 and 5.5 Vp for transmitted logic one
- F. **Input Facility Impedance:** 135 Ohms @ 64 Kb/s.
- G. **Power:** -48 VDC -5 VDC, and +5 VDC supplies.
- H. **Power Consumption:** 0.4 Watts, nominal

Model	Description
AUA234CI3	SLC-5/SLC-2000 Intelligent All-Rate DS0 Dataport. CLEI* Code: 5SC6STSBAA. Barcode: 117593. CPR: B73761.

\*CLEI is a trademark of Telcordia Technologies.

**Table 5. Ordering Information**